Electronic Version
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Claims

[c1] What is claimed is:

1. A method for locking phase by providing a clock synchronized with an input signal,the input signal comprising a plurality of data, the method comprising:
generating an estimated rate according to transitions of the input signal;
processing a dithering step for updating the estimated rate by multiplying the estimated rate by a predetermined ratio;
adjusting a frequency of the clock synchronized with an input signal according to the updated estimated rate in the dithering step to make the frequency of the clock correspond to the updated estimated rate; and
modifying the predetermined ratio so that another dithering step may apply the modified predetermined ratio to update the estimated rate.

[c2] 2. The method of claim 1 wherein the predetermined ratio will not vary with the change of the estimated rate in the dithering step when processingthe dithering step.

[c3] 3. The method of claim 1 further comprising changing the predetermined ratiosof the adjacent dithering steps

according to a predetermined rule.

[c4] 4. The method of claim 1 further comprising:
obtaining a sampling clock wherein the sampling clock comprises a plurality of sampling cycles;
generating the input signal according to a signal level of a data signal corresponding to the sampling cycles in the sampling clock; and
generating the estimated rate according to the number of the sampling cycles in a predetermined period of time and the number of the changes of the signal level of the input signal in the predetermined period of time.

[c5] 5. The method of claim 1 wherein before adjusting the frequency of the clock according to the updated estimate rate in the dithering step, a judgment step is processed according to a phase difference or frequency difference between the clock and the input signal to decide whether the frequency of the clock is adjusted according to the updated estimated rate in the dithering step.

[c6] 6. The method of claim 5 wherein in the judgment step, if the phase difference or the frequency difference between the clock and the input signalexceeds a predetermined value, the frequency of the clock is adjusted according to the updated estimated rate in the dithering step.

[c7] 7. The method of claim 5 wherein in the judgment step, if the phase difference or the frequency difference between the clock and the input signalis lower than a predetermined value, the frequency of the clock is not adjusted according to the updated estimated rate in the dithering step.

[c8] 8. A phase lock circuit for providing a clock synchronized with an input signal, the input signal comprising a plurality of data, the phase lock circuit comprising:
a measuring module for generating an estimated rate according to transitions of the input signal;
a dithering module coupled to the measuring module for updating the estimated rate by multiplying the estimated rate by a predetermined ratio; and
an oscillator for adjusting a frequency of the clock synchronized with an input signal according to the updated estimatedrate in the dithering module to make the frequency of the clock correspond to the updated estimatedrate;
wherein after the dithering module updates the estimatedrate, the predetermined ratio is modified to multiply the estimated rate by a modified predetermined ratio for updating the estimated rate in the dithering modulewhenthe dithering module generates another updated estimatedrate.

[c9] 9. The phase lock circuit of claim 8 wherein the predetermined ratio of the dithering module will not vary with the change of the estimated rate of the measuring module.

[c10] 10. The phase lock circuit of claim 8 wherein the dithering module modifies the predetermined ratio after the estimated rate is updated according to a predetermined rule, so that the modified predetermined ratio can be used when the estimated rate is updated the next time.

[c11] 11. The phase lock circuit of claim 8 further comprising:
a converter for receiving a sampling clock that comprises a plurality of sampling cycles and for generating the input signal according to a signal level of a data signal corresponding to the sampling cycles in the sampling clock;
wherein the measuring module generates the estimated rate according to the number of the sampling cycles in a predetermined period of time and the number of the changes of the signal level of the input signal.

[c12] 12. The phase lock circuit of claim 8 further comprising a detecting circuit for deciding whether the updated estimated rateof the dithering module is transmitted to the oscillator to adjust the frequency of the clock according

to a phase difference or frequency difference between the clock and the input signal.

[c13] 13. The phase lock circuit of claim 12 wherein if the detecting circuit detects that the phase difference or the frequency difference between the clock and the input signalexceeds a predetermined value, the updated estimated rateof the dithering module is transmitted to the oscillator.

[c14] 14. The phase lock circuit of claim 13 further comprising an error-test module for generating a frequency adjustment value according to the phase difference or the frequency difference between the clock and the input signalwherein when the phase difference or the frequency difference between the clock and the input signalis lower than a predetermined value, theupdated estimated rateof the dithering module ceases to be transmitted to the oscillator and the frequency adjustment value of the error-test module is transmitted to the oscillator,so that the oscillator can adjust the frequency of the clock according to the frequency adjustment value.

[c15] 15. A method for locking phase by providing a comparing clock synchronized with an input signal,the input signal comprising a plurality of data, the method comprising:

generating a frequency adjustment value according to the input signal; generating a dithering estimated value according to the input signal through a dithering step; setting a dithering estimated value as a new comparing clock when a synchronization error between the comparing clock and the input signal exceeds a predetermined value; and

comparing the new comparing clock with the input signal in order to adjust the new comparing clock.

[c16] 16. The method of claim 15 wherein the dithering step is used to generate an estimated rate according to transitions ofthe input signal and to generate the dithering estimated value by multiplying the estimated rate by a predetermined ratio.

[c17] 17. The method of claim 16wherein the predetermined ratio will not vary with the change of the estimated rate in the dithering step.

[c18] 18. The method of claim 16 wherein the predetermined ratio of the adjacent dithering step is changed according to a predetermined rule.

[c19] 19. The method of claim 15 further comprising adjusting the frequency of the comparing clock according to a phase difference or frequency difference between the

comparing clock and the input signal.

[c20] 20. The method of claim 15further comprising:
generating an estimated rate according to the number of sampling cycles in a predetermined period of time and the number of the changes of signal level of the input signal in the predetermined period; and
generating the dithering estimated value in the dithering step according to the estimated rate.